New Measurement-Based Technique for RF LDMOS Nonlinear Modeling

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***Abstract*—In this letter a new look-up table model is developed for the nonlinear modeling of radio frequency (RF) LDMOS transistors. The modeling technique is based on the use of approximation splines that are coupled to a pulsed *I–V* characterization setup. It provides a very fast modeling procedure, while avoiding the appearance of undesired ripples in the modeled functions. The technique has been applied to a RF LDMOS technology for *L*-band applications, obtaining excellent results in the prediction of both the small- and large-signal transistor responses. This technique is specially suitable for fast-evolution technologies.**

***Index Terms*— Cubic B-splines, LDMOS transistors, look-up table model, nonlinear modeling.**

I. Introduction

THE technology for microwave and radio-frequency (RF) active devices is evolving rapidly in order to meet the needs of today's radio-mobile applications. Nonlinear models become obsolete fast and must be continuously readapted to the technological changes. Thus, it is necessary to have model extraction techniques that are simple and fast while maintaining accuracy. RF LDMOS transistors play a major role in L-band power amplification [1]. When applied to RF power LDMOS, traditional semiempirical MOSFET models require the use of additional parameters, which excessively complicates the model extraction [2]. On the other hand, look-up table models seem a suitable choice for rapidly evolving technologies, since there is no need for any parameter extraction process. Classical look-up table models, however, commonly make use of cubic splines as interpolation tool, which can give rise to unwanted ripples in the modeled functions [3]. Therefore, the model derivatives are not correctly represented, leading to a wrong prediction of the device small-signal responses. The interpolation of the measurement noise inherent in any characterization system aggravates this undesirable effect. This can be particularly inconvenient for the design of ultralinear amplifiers where very low power levels are involved. An attractive method to cope with this problem was recently presented in [4]. Here, a different approach is proposed. It is based on the use of cubic B-splines [5] that are not forced to pass through the measurement points. These "approximation" splines are coupled to a nonuniform distribution of the measurement data that concentrates the points in the strongly nonlinear regions. For that purpose, specific algorithms have been developed in order to get the optimal measurement distribution that ensures accuracy while avoiding unwanted ripples.

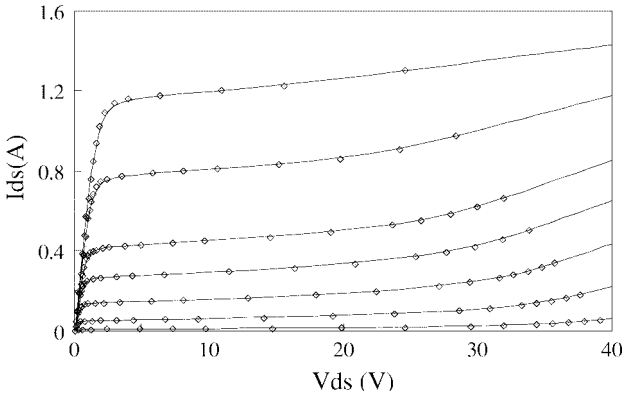

Fig. 1. Drain–current characteristics of the LDMOS LV1 transistor. Dots: pulsed I–V measurements. Solid lines: new look-up table model.

In addition, it is important to notice that look-up table models can only provide reliable simulations results within the regions that have been characterized. In power applications, the device may explore regions that are outside the safe operation area (SOA) during its normal operation. Therefore, a set of measurement data suitable for look-up table modeling of power LDMOS must include the high-power dissipation region and the breakdown region. Hence, the use of a pulsed I–V characterization that allows the safe characterization of these regions is proposed here.

The technique has been applied to a LDMOS technology for power amplification in L band. An accurate prediction of the small signal response have been obtained. The accuracy of the large-signal simulations has been successfully verified by means of load–pull measurements.

II. Look-Up Table Model

Let $y(x)$ be the function to be modeled from a series of measurement data points $y_i(x_i)$. An auxiliary interpolation parameter u is used corresponding to the order of the data in the series $(u_i = 1, 2, 3, \cdots, n)$. The functions that are actually interpolated are $y(u)$ and $x(u)$. Then, the desired $y(x)$ function is obtained from the combination of $y(u)$ and $x(u)$. The base functions that have been chosen are approximation cubic B-splines. For $u_i < u < u_{i+1}$, the base functions are expressed

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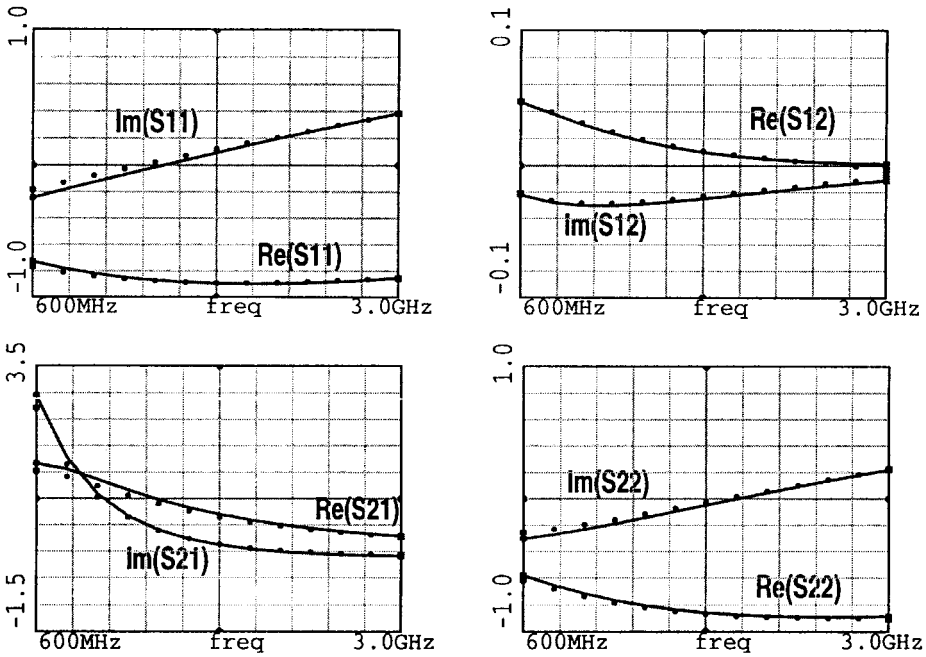

Fig. 2. S-parameters of the LDMOS LV1 transistor for $V_{\rm ds} = 6$ V, $V_{\rm gs} = 1.8$ V. Dots: measurements. Solid line: obtained from a harmonic-balance simulation of the nonlinear model.

as

$$\begin{aligned} B_0(u) &= -\tfrac{1}{6}(u-u_i)^3 + \tfrac{1}{2}(u-u_i)^2 - \tfrac{1}{2}(u-u_i) + \tfrac{1}{6} \\ B_1(u) &= \tfrac{1}{2}(u-u_i)^3 - (u-u_i)^2 + \tfrac{2}{3} \\ B_2(u) &= -\tfrac{1}{2}(u-u_i)^3 + \tfrac{1}{2}(u-u_i)^2 + \tfrac{1}{2}(u-u_i) + \tfrac{1}{6} \\ B_3(u) &= +\tfrac{1}{6}(u-u_i)^3 \end{aligned} \tag{1}$$

and the $y(u)$ and $x(u)$ functions are approximated by

$$y(u) = \sum_{k=0}^{3} y_{i+k} B_k(u); \quad x(u) = \sum_{k=0}^{3} x_{i+k} B_k(u). \tag{2}$$

Equation (2) can be generalized for a two-dimensional set of measurement points $z_{i,j}(u_i, v_j)$. In this case, for $u_i < u < u_{i+1}$ and $v_j < v < v_{j+1}$, the z function is approximated by

$$z(u, v) = \sum_{l=0}^{3} \sum_{k=0}^{3} z_{i+k,\, j+l} B_k(u) B_l(v). \tag{3}$$

In our representation, three functions are approximated as a function of two auxiliary parameters u and v, corresponding to the order of the data points in $V_{\rm ds}$ and $V_{\rm gs}$, respectively:

$$V_{\rm ds} = V_{\rm ds}(u) \quad V_{\rm gs} = V_{\rm gs}(v) \quad I_{\rm ds} = I_{\rm ds}(u, v). \tag{4}$$

The three functions in (4) are combined in order to obtain the drain current model $I_{\rm ds} = I_{\rm ds}(V_{\rm ds}, V_{\rm gs})$. The use of the auxiliary parameters (u, v) allows a nonuniform distribution of the measurement points in $V_{\rm ds}$ and $V_{\rm gs}$, which is essential for controlling model accuracy. The resulting model has a C2 continuity which avoids convergence problems in harmonic balance software. The main feature of this tool is that the splines do not pass through the measurement points but only approximate them, avoiding the interpolation of noisy measurement data. The accuracy of the approximation depends on the measurement data distribution and, because of the local nature of the representation, this can be controlled locally by adding new measurement points. Therefore, a specific recursive algorithm has been developed to drive the measurement data acquisition of the pulsed I–V setup. Each time a new measurement point is added, an estimation of the accuracy in all the model regions is carried out. Quasi-linear regions only need a few points to be represented accurately. On the contrary, strongly nonlinear regions must be represented by a higher number of points in order to achieve the desired accuracy. The final result is a measurement distribution that concentrates the points in the nonlinear regions while keeping a small number of points in the quasi-linear regions. This significantly lowers the risk of undesirable ripples in the modeled functions.

The measurement data set provided by the pulsed I–V setup directly feeds the look-up table model of the drain current. To obtain a nonlinear model for a different transistor only a new characterization is needed and the nonlinear model for the drain current follows straightforward.

III. Results

The proposed technique has been applied to a medium power LDMOS transistor (LDMOS LV1 technology) currently used in RF power applications. The model has been implemented in a harmonic balance commercial simulator. A classical field effect topology was chosen with the drain current $I_{\rm ds}(V_{\rm ds}, V_{\rm gs})$ being the only nonlinear element [6]. The rest of elements of the topology have been extracted from S-parameter measurements as proposed in [6]. Fig. 1 superimposes the resulting look-up table model for the drain current source to the pulsed I–V measurement results. Note the excellent accuracy of the approximation and how the measurement points accumulate in the nonlinear zones.

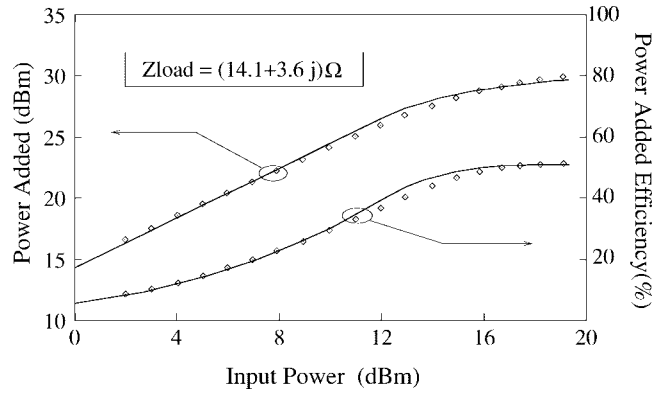

Fig. 3. LDMOS LV1 transistor. Added power PA and power-added efficiency PAE at 1 GHz. AB class bias conditions ($V_{\rm ds0} = 6$ V, $I_{\rm ds0} = 80$ mA). Dots: load–pull measurements. Solid line: harmonic balance simulation.

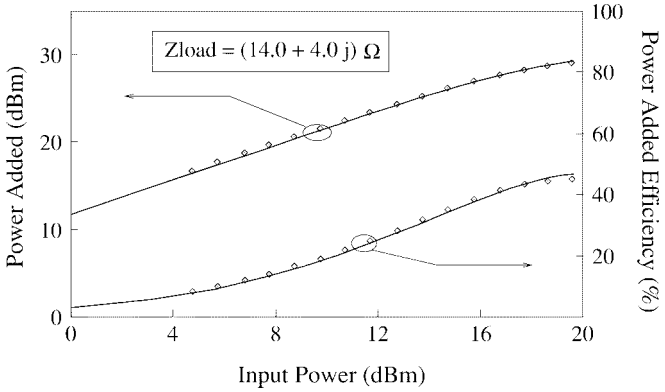

Fig. 4. LDMOS LV15 transistor. Added power PA and power-added efficiency PAE at 1 GHz. AB class bias conditions ($V_{\rm ds0} = 6$ V, $I_{\rm ds0} = 80$ mA). Dots: load–pull measurements. Solid line: harmonic balance simulation.

In order to verify that the model is suitable for the simulation of the device responses when very low power levels are involved, several comparisons between the measured and simulated S-parameters were carried out covering the whole ($V_{\rm ds}$, $V_{\rm gs}$) range. The measurements of the S-parameters were performed under pulsed bias conditions. The simulated S-parameters were obtained from a harmonic balance analysis, i.e., making use of the nonlinear look-up table model. The results obtained for a particular bias point are shown in Fig. 2. Similar results were obtained for different bias points. The good agreement confirms that model derivatives are realistic and accurate allowing a correct prediction of the small-signal behavior of the LDMOS.

Next, the accuracy in the large signal simulation was analyzed. To do so, active load–pull measurements were performed and successfully compared with simulation results. As an example, Fig. 3 shows the added power PA and the power-added efficiency PAE as a function of the input power $P_{\rm in}$ for a AB class at 1 GHz. Note that excellent accuracy is found for the whole $P_{\rm in}$ range. This includes the very low $P_{\rm in}$ level where traditional look-up table models fail to predict correctly the device response. Additional comparisons were performed for different operation classes, frequencies, and load conditions, obtaining similar results. Furthermore, a technological variant of the previous LDMOS was also analyzed (LDMOS LV15 technology). The corresponding drain current nonlinear model was directly obtained from a new characterization in less than 30 min. Again, an excellent agreement was found between nonlinear simulations and load–pull results (Fig. 4).

IV. Conclusion

In this paper a new measurement-based technique is presented for the nonlinear modeling of RF LDMOS devices. It is based on the use of approximation splines that avoid the interpolation of noisy measurement data. The model is coupled to a pulsed I–V measurement setup that allows the characterization outside the SOA regions. This measurement system provides an efficient data distribution that ensures model accuracy while minimizing the presence of ripples in the modeled functions. The new technique takes advantage of the fast modeling procedure typical of look-up table models while ensuring an accurate prediction of both the small- and large-signal responses of the device. The model has been validated for a LDMOS technology currently used in radio mobile applications. Due to its straightforward and simple nature, the proposed technique seems specifically suitable for technologies that evolve rapidly.

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